HTG19264A-35W-36K08-V01

产品名称（**Product name**）	:	黑白点阵 COG
型　　号（**Model**）	:	HTG19264A-35W-36K08-V01
编　　号（**EDC number**）	:	10200425
日　　期（**Date**）	:	2018-01-18

编码：QR-R-011　A/0　　序号：

深圳市鑫洪泰电子科技有限公司 **Shenzhen Hot Display Technology Co.,Ltd**		
编制 **Prepared by**	审核 **Checked by**	核准 **Approved by**

Rev.	Descriptions	Date
01	Prelimiay Release	2018-01-22
02		

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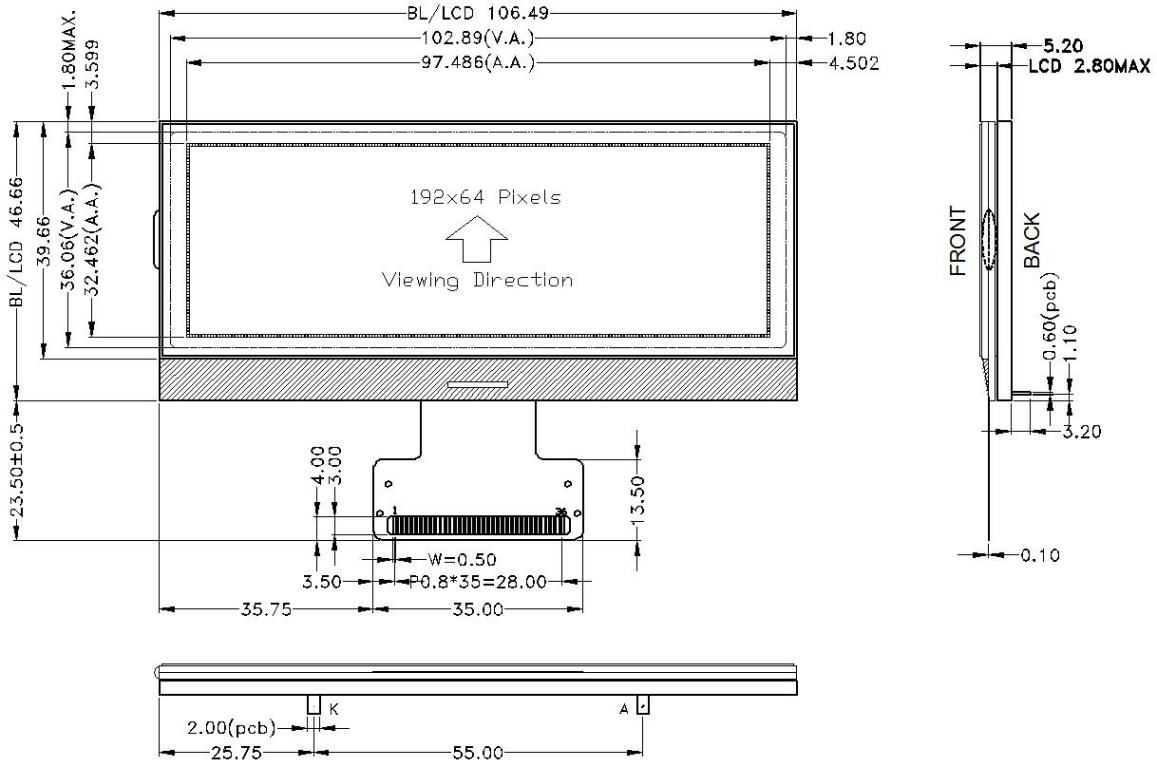
1. Bsaic Specifications

1.1 Display Specifications

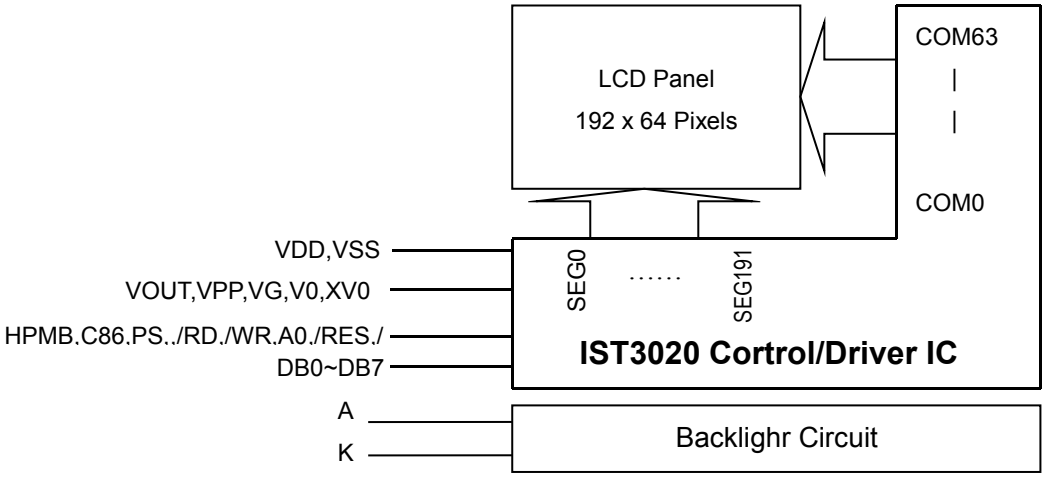
1>LCD Display Mode : FSTN, Positive, Transmissive
2>Viewing Angle : 6H
3>Driving Method : 1/64 Duty, 1/9 Bias
4>Backlight : White LED

1.2 Mechanical Specifications

1>Outline Dimension : 106.49x46.6 x 5.2mm (See attached Outline Drawing for Details)



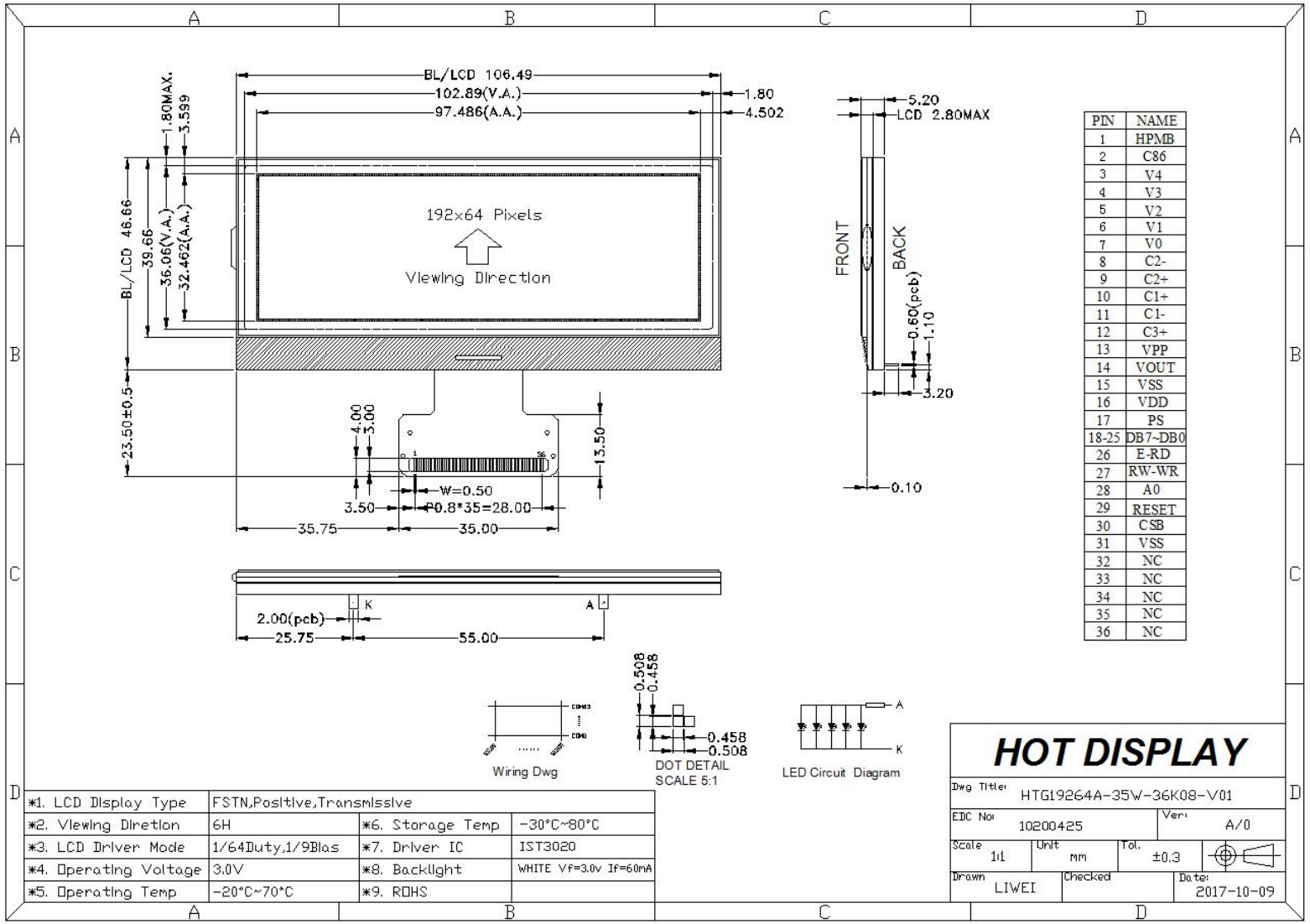
1.3 Circuit Diagram



1.4 Terminal Function

Pin No.	Pin Name	Function
1	HPMB	Power supply control pin of the power supply circuit for LCD driver - HPMB = “H” : Normal mode - HPMB = “L” : High power supply mode
2	C86	This is the MPU interface selection pin. C86 = “H”: 6800 Series MPU interface. C86 = “L”: 8080 Series MPU interface.
3-7	V4,V3,V2,V1,V0	LCD driving voltages.
8-12	C2-,C2+,C1+,C1-,C3+,	DC/DC voltage converter
13	VPP	VPP is the power pin of embedded OTP (One-Time Programming) non-volatile memory circuit.
14	VOUT	Voltage converter input / output pin Connect this pin to VSS through capacitor.
15	VSS	Negative power supply,0V
16	VDD	Power supply voltage (Positive)
17	PS	This pin configures the interface to be parallel mode or serial mode. P/S = “H”: Parallel data input/output. P/S = “L”: Serial data input.
18-25	DB7-DB0	DC/DC voltage converter.
26	E-RD	Read (/RD) control signal input.
27	RW-WR	Write (/WR) control signal input.
28	A0	Register select input pin - A0 = “H” : DB0 to DB7 are display data - A0 = “L” : DB0 to DB7 are control data
29	RESET	Rester Pin(L->H)
30	CSB	This is the chip select signal.
31	VSS	Negative power supply,0V
32-36	NC	NC

1.5 Product Outline



PIN	NAME
1	HPMB
2	C86
3	V4
4	V3
5	V2
6	V1
7	V0
8	C2-
9	C2+
10	C1+
11	C1-
12	C3+
13	VPP
14	VOUT
15	VSS
16	VDD
17	PS
18-25	DB7~DB0
26	E-RD
27	RW-WR
28	A0
29	RESET
30	CSB
31	VSS
32	NC
33	NC
34	NC
35	NC
36	NC

*1. LCD Display Type	FSTN,Positive,Transmissive		
*2. Viewing Direction	6H	*6. Storage Temp	-30°C~80°C
*3. LCD Driver Mode	1/64Duty,1/9Bias	*7. Driver IC	IST3020
*4. Operating Voltage	3.0V	*8. Backlight	WHITE Vf=3.0v If=60mA
*5. Operating Temp	-20°C~70°C	*9. ROHS	

2. Absolute Maximum Ratings

Items	Symbol	MIN.	MAX.	Unit	Condition
Supply Voltage	VDD	-0.3	+3.6	V	Vss = 0V
Input Voltage	VIN	-0.3	VDD+0.3	V	Vss = 0V
Operating Temperature	TOP	-20	+70	℃	No Condensation
Storage Temperature	Tst	-30	+80	℃	No Condensation

3. Electrical Characteristics

3.1 DC Characteristics

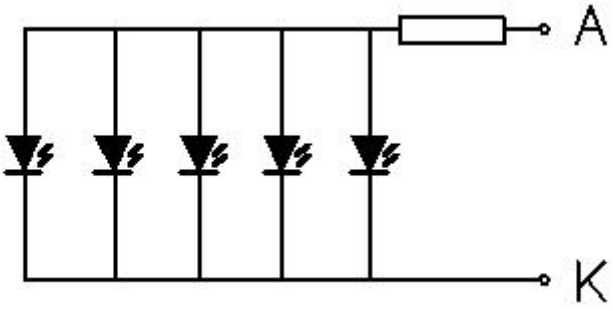
Vss = 0V,Top = 25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Operating Voltage	VDD	3.0	3.3	3.6	V	VDD
Input High Voltage	VIH	0.8 x VDD	-	VDD	V	/CS1,/RES,A0,/WR, /RD,D0~D7,C86
Input Low Voltage	VIL	Vss	-	0.2 x VDD	V	
Output High Voltage	VOH	0.8 x VDD	-	VDD	V	D0~D7
Output Low Voltage	VOL	Vss	-	0.2 x VDD	V	D0~D7
Input Leakage Current	ILI	-1.0	-	1.0	μA	VDD
Output Leakage Current	ILo	-3.0	-	3.0	μA	VDD

3.2 LED Backlight Circuit

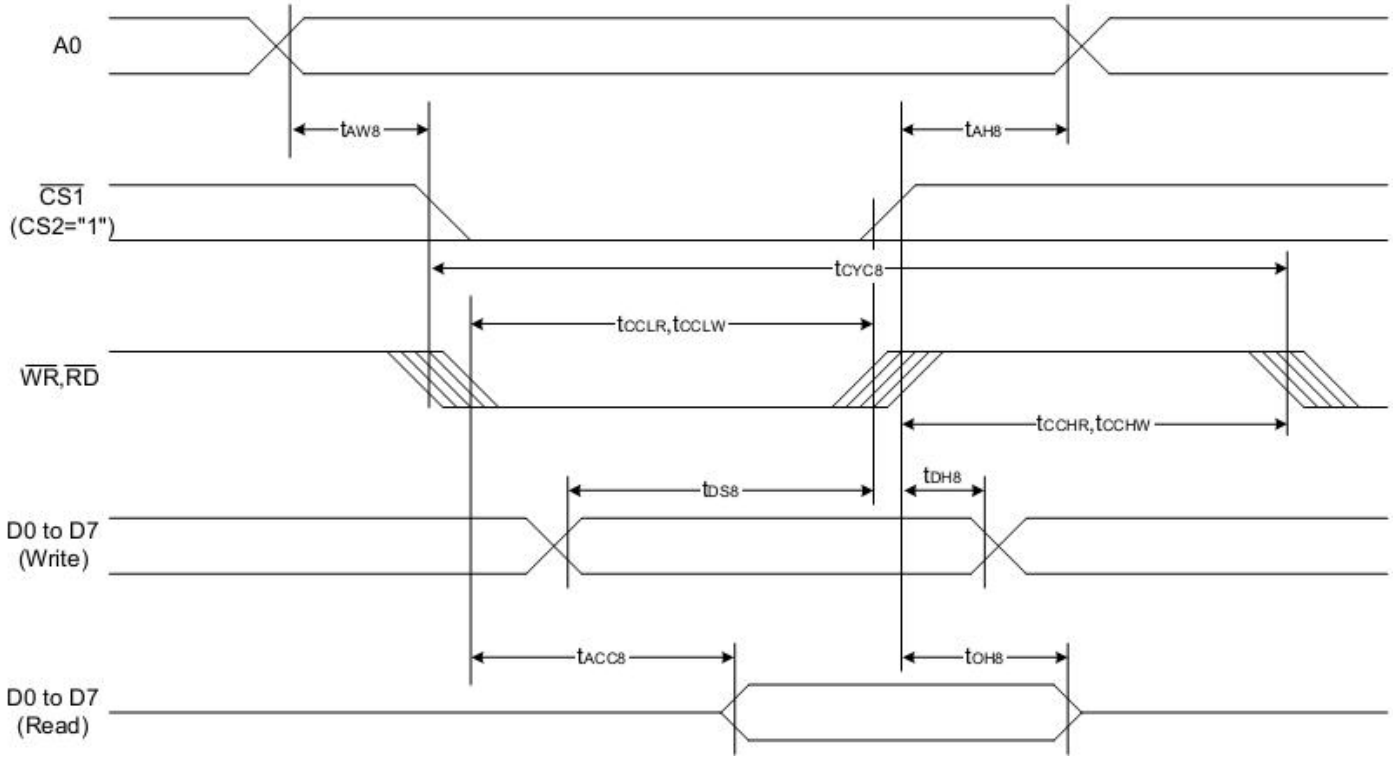
Vss = 0V,Top = 25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Forword Voltage	Vf BLA	-	3.1	-	V	VDD
Forword Current	If BLA	-	75	90	mA	VDD



3.3 AC Characteristics

3.3.1 8080 Mode System Bus Timing



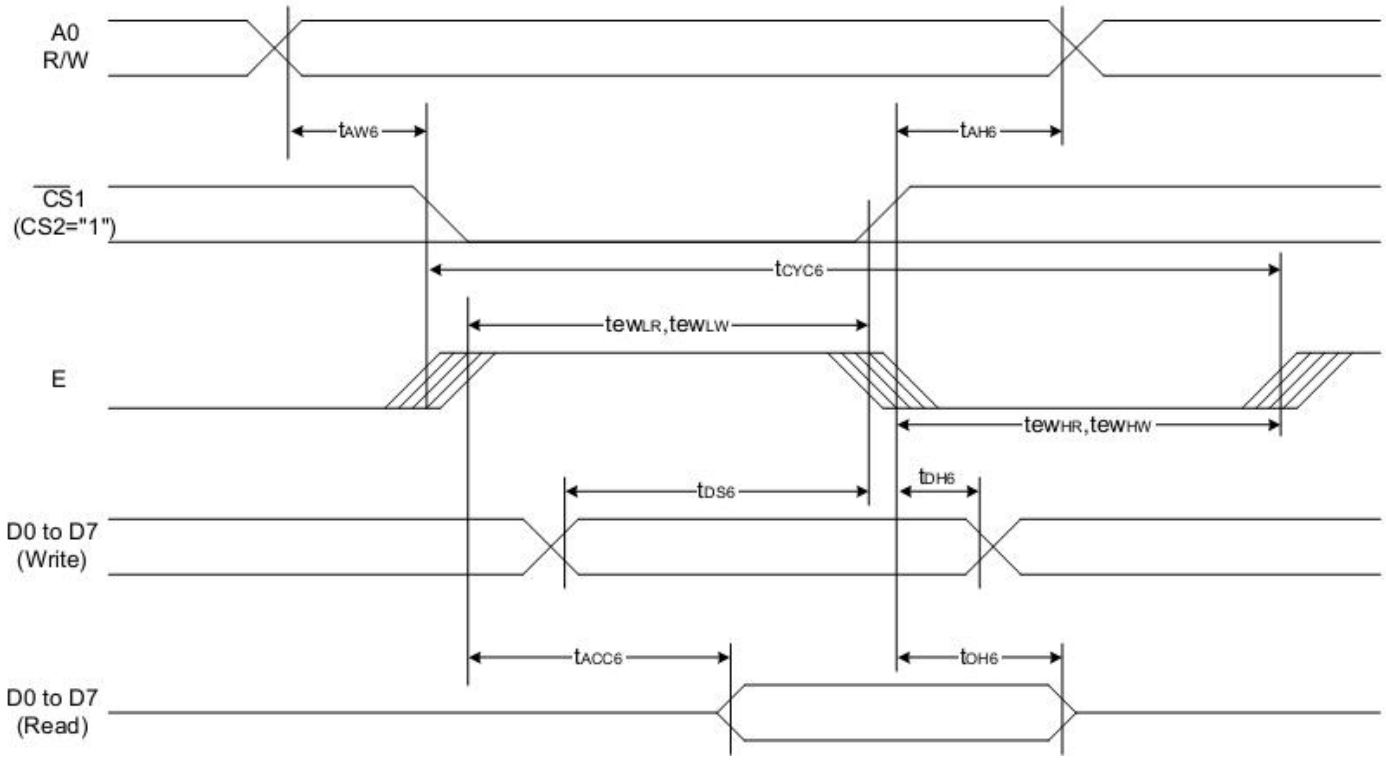
Vss = 0V,Top = 25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
System cycle time	Tcyc8	300	-	-	ns	-
Address setup time(A0)	Taw8	0	-	-	ns	-
Address hold time(A0)	Tah8	0	-	-	ns	-
Control Low Pulse wide(/RD)	tcclr	275	-	-	ns	-
Control Low Pulse wide(/WR)	tcclw	275	-	-	ns	-
Control High Pulse wide(/RD)	tcchr	225	-	-	ns	-
Control High Pulse wide(/WR)	tcchw	225	-	-	ns	-
Data steup time	Tds8	40	-	-	ns	-
Data hold time	Tdh8	10	-	-	ns	-
/RD access time(*a)	Tacc8	-	-	200	ns	-
Output disable time(*a)	Tch8	15	-	150	ns	-

Note:

***a. all timing is using 20％ and 80％ of VDD as the reference.**

3.3.2 6800 Mode System Bus Timing



Vss = 0V,Top = 25℃

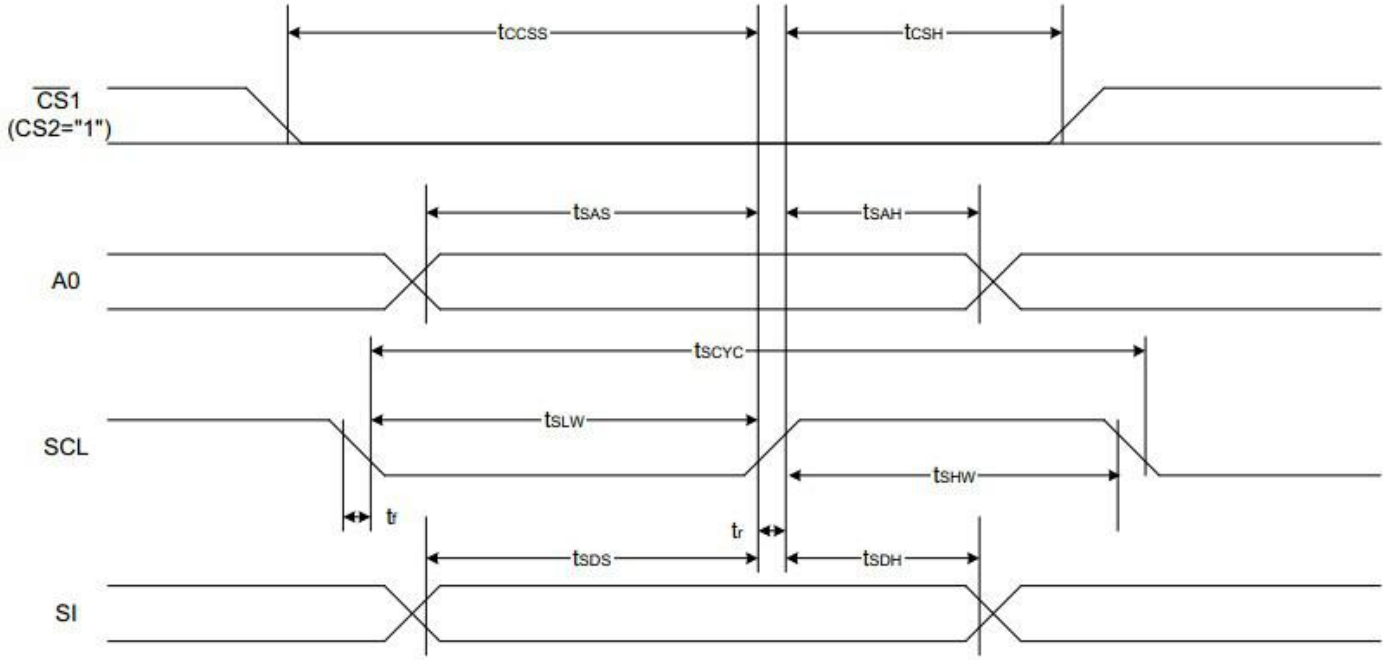
Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
System cycle time	Tcyc6	300	-	-	ns	-
Address setup time(A0)	Taw6	0	-	-	ns	-
Address hold time(A0)	Tah6	0	-	-	ns	-
Control Low Pulse wide(/RD)	tcclr	275	-	-	ns	-
Control Low Pulse wide(/WR)	tcclw	275	-	-	ns	-
Control High Pulse wide(/RD)	tcchr	225	-	-	ns	-
Control High Pulse wide(/WR)	tcchw	225	-	-	ns	-
Data steup time	Tds6	40	-	-	ns	-
Data hold time	Tdh6	10	-	-	ns	-
/RD access time(*a)	Tacc6	-	-	200	ns	-
Output disable time(*a)	Tch6	15	-	150	ns	-

Note:

***a. all timing is using 20％ and 80％ of VDD as the reference.**

***b. CL = 100pF**

3.3.3 4-line SPI Mode



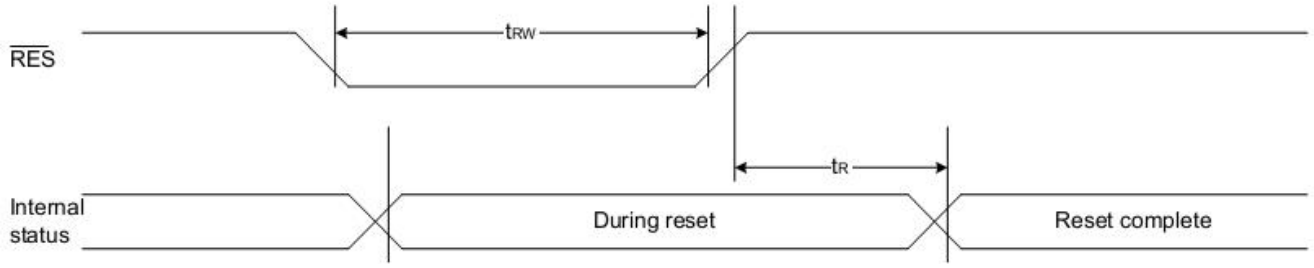
(V_{DD} = 3.3V, Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	T_{scyc}		50	—	ns
SCL "H" pulse width		T_{shw}		25	—	
SCL "L" pulse width		T_{SLW}		25	—	
Address setup time	A0	T_{SAS}		20	—	
Address hold time		T_{sah}		10	—	
Data setup time	SI	T_{sds}		20	—	
Data hold time		T_{SDH}		10	—	
CS-SCL time	CS	T_{css}		20	—	
CS-SCL time		T_{csh}		40	—	

(V_{DD} = 1.8V, Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	T_{SCYC}		200	—	ns
SCL "H" pulse width		T_{SHW}		80	—	
SCL "L" pulse width		T_{SLW}		80	—	
Address setup time	A0	T_{SAS}		60	—	
Address hold time		T_{SAH}		30	—	
Data setup time	SI	T_{SDS}		60	—	
Data hold time		T_{SDH}		30	—	
CS-SCL time	CS	T_{CSS}		40	—	
CS-SCL time		T_{CSH}		100	—	

3.4 Reset Timing



(VDD = 3.3V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.0	us
Reset "L" pulse width	/RES	tRW		1.0	—	—	us

Table 37

(VDD = 2.7V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset "L" pulse width	/RES	tRW		2.0	—	—	us

Table 38

(VDD = 1.8V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	3.0	us
Reset "L" pulse width	/RES	tRW		3.0	—	—	us

Note:

***a. all timing is using 20％ and 80％ of VDD as the reference.**

4. Function specifications

4.1 The Parallel Interface

Shared	6800 Mode		8080 Mode		Function
A0	R/W	E	/RD	/WR	
H	H	H	L	H	Reads the display data
H	L	H→L	H	L → H	Writes the display data
L	H	H	L	H	Staus read
L	L	H→L	H	L → H	Write Command data

NOTE: if SPI be used, C86=0,P/S=0;

4.2 Basic Setting

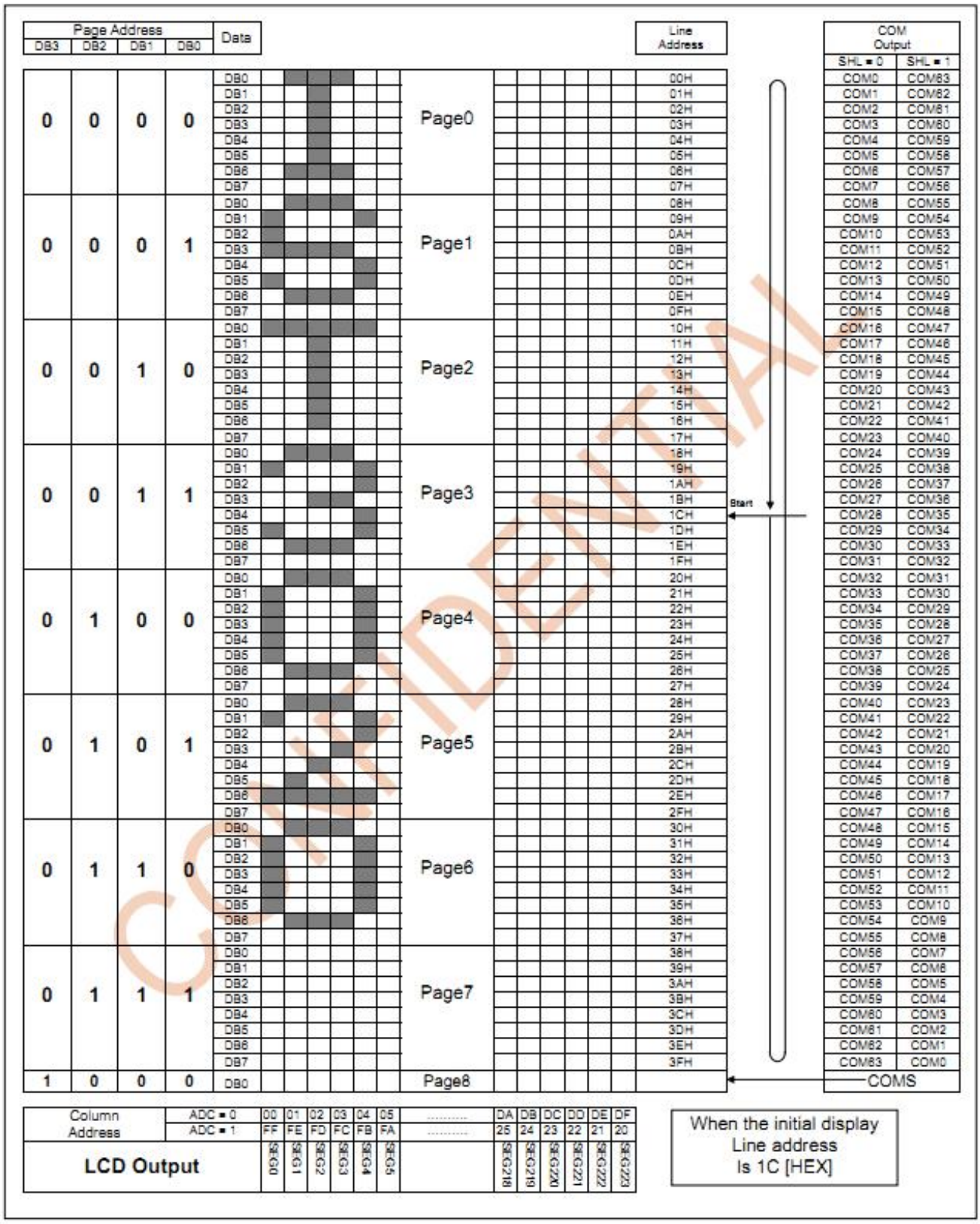
To drive the LCD module correctly and provide normally display, please use the following seting

1> ADC = 0 (normal)
2> SHL select = 1(reverse)
3> LCD Bias Select = 1/9
4> Initial Display Line = 0
5> Entire Display ON/OF = OFF(normal)
6> Reverse Display ON/OF = OFF(normal)
7> Set Power Control Set:
Voltage follower = ON,voltage converter = ON,Voltage regulator = ON
8> Display ON/OF =ON

4.3 Resetting the LCD module

The LCD module should be initialized bu using /RES terminal.
While turning on the VDD and VSS power supply, maintain /RES terminal at LOW level, After the Power supply stabilized, release the reset terminal(/RES = High)

4.4 Display Memory Map



4.5 Display Commands

× : Don't care

INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn on/off LCD panel When DON = 0 : display OFF When DON = 1 : display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Read status	0	1	BUSY	ADCB	ON/OFF	RESETB	0	0	0	0	Read the internal status
Write display data	1	0	Write data								Write data into DDRAM
Read display data	1	1	Read data								Read data from DDRAM
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC = 0 : normal direction (SEG0 → SEG223) when ADC = 1 : reverse direction (SEG223 → SEG0)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0 : normal display When REV = 1 : reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal / entire display ON When EON = 0 : normal display When EON = 1 : entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL = 0 : normal direction (COM0 → COM63) When SHL = 1 : reverse direction (COM63 → COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	0	0	1	0	1	0	1	0	0	SAV	Select power save mode When SAV = 0 : Stand-by When SAV = 1 : Sleep
Power save reset	0	0	1	1	1	0	0	0	0	1	Reset power save
Set n-Line reversal drive register	0	0	0	0	1	1	NL3	NL2	NL1	NL0	Set the number of line reversal drive line

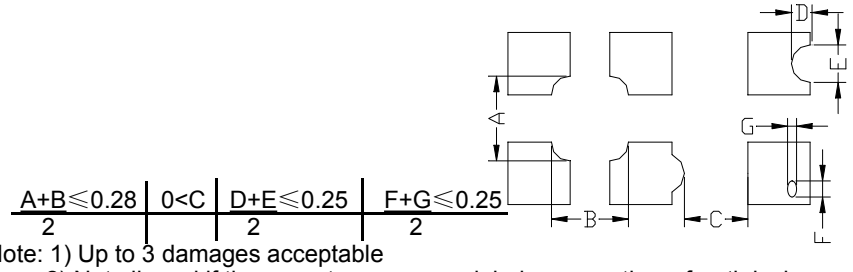
n-Line reversal drive reset	0	0	1	1	1	0	0	1	0	0	Reset the line reversal drive
Built-in oscillator ON	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator circuit
External capacitor discharge	0	0	0	1	1	1	0	DISC			DISC = 000 (enable) DISC = 111 (disable)
NOP	0	0	1	1	1	0	0	0	1	1	Non-Operation command
Test	0	0	1	1	1	1	×	×	×	×	Don't use this instruction
Set OTP program	0	0	1	0	0	1	0	0	0	0	Set OTP program mode
OTP program control	0	0	OTPADJ	OTPPON	x	x	x	x	x	x	OTP control option OTPADJ = 1:OTP use OTPADJ = 0:OTP ignore OTPPON =1:OTP program enable OTPPON = 0:OTP program disable
Set contrast offset (1)	0	0	1	0	0	1	0	0	0	1	Set contrast offset mode (1)
	0	0	×	×	CTA5	CTA4	CTA3	CTA2	CTA1	CTA0	Set contrast offset register (1)
Set contrast offset (2)	0	0	1	0	0	1	0	0	1	0	Set contrast offset mode (2)
	0	0	×	×	×	CTB4	CTB3	CTB2	CTB1	CTB0	Set contrast offset register (2)
Set contrast offset (3)	0	0	1	0	0	1	0	0	1	1	Set contrast offset mode (3)
	0	0	×	×	×	CTC4	CTC3	CTC2	CTC1	CTC0	Set contrast offset register (3)
Read contrast offset(1)	0	0	1	0	0	0	1	1	0	0	Set contrast offset read mode (1)
	0	1	x	x	CTA5	CTA4	CTA3	CTA2	CTA1	CTA0	Read contrast offset(1)
Read contrast offset(2)	0	0	1	0	0	0	1	1	0	1	Set contrast offset read mode (2)
	0	1	x	x	x	CTB4	CTB3	CTB2	CTB1	CTB0	Read contrast offset(2)
Read contrast offset(3)	0	0	1	0	0	0	1	1	1	0	Set contrast offset read mode (3)
	0	1	x	x	x	CTC4	CTC3	CTC2	CTC1	CTC0	Read contrast offset(3)

4.6 Basic Operating Sequence

Initialization Sequence

	Code Function										Note
	A0	D7	D6	D5	D4	D3	D2	D1	D0	hex	
Turn on Power Supply VDD & VSS While maintaining /RES at LOW	-	-	-	-	-	-	-	-	-	-	-
Wait until power supply is stabilized	-	-	-	-	-	-	-	-	-	-	-
Release the /RES Reset Signal (/RES = High)	-	-	-	-	-	-	-	-	-	-	See AC Characteristics section for timing details
LCD Bias = 1/9	0	1	0	1	0	0	0	1	0	A2H	LCD Characteristics
ADC = Normal	0	1	0	1	0	0	0	0	0	A0H	No flip on x-direction (SEG)
SHL = Reverse	0	1	1	0	0	1	0	0	0	C8H	Flip on y- direction (COM)
Initial Display Line = 0	0	0	1	0	0	0	0	0	0	40H	i.e. Display RAM “Page 0-D0” Matched to top line of the LCD
Power Control Voltage Follower = OFF Voltage Regulator = OFF Voltage Converter = ON	0	0	0	1	0	1	1	0	0	2CH	Turn on the internal Voltage Converter and wait until VOUT stable
Delay 50ms	-	-	-	-	-	-	-	-	-	-	
Power Control Voltage Follower = OFF Voltage Regulator = OFF Voltage Converter = ON	0	0	0	1	0	1	1	1	0	2EH	Turn on the internal Voltage Regulator and wait until VOUT stable
Delay 50ms	-	-	-	-	-	-	-	-	-	-	
Power Control Voltage Follower = OFF Voltage Regulator = OFF Voltage Converter = ON	0	0	0	1	0	1	1	1	1	2FH	Turn on the internal Voltage Follower and wait until VOUT stable
Delay 50ms	-	-	-	-	-	-	-	-	-	-	
Regulator Resistor Select	0	0	0	1	0	0	1	0	1	25H	Set the built-in resistor ratio to middle
Set Reference Voltage Mode	0	1	0	0	0	0	0	0	1	81H	Set to the middle of the range it may be adjused
Set Reference Voltage Resistor	0	0	0	1	0	0	0	1	0	22H	For achieving the best display contrast
Display ON	0	1	0	1	0	1	1	1	1	AFH	Turn on the LCD display
Set Page Address = 0	0	1	0	1	1	0	0	0	0	B0H	Specify the display data RAM page address to 00H
Set Column Address (Upper -4bit = 0)	0	0	0	0	1	0	0	0	0	10H	Specify the display data RAM column address to 00H
Set Column Address (Lower-4bit =4)	0	0	0	0	0	0	1	0	0	00H	
Write Display Data	1	Display Data									-
Write Other Display Data											

5. Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2}\leq 0.28$ | 0<C | $\frac{D+E}{2}\leq 0.25$ | $\frac{F+G}{2}\leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with “2) Black/white spot”, and “3) Black/White line”.	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball, solder hips)	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm) (3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	Minor
16) Bezel flaw	Bezel claw missing or not bent	Minor
17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor

6. Handling Precautions

6.1 Mounting method

A panel of LCD module made by our company consists of two thin glass plates with polarizers that easily get damaged.

And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB), extreme care should be used when handling the LCD modules.

6.2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

-Isopropyl alcohol

-Ethyl alcohol

-Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

-Water

-Ketene

-Aromatics

6.3 Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

6.4 Packaging

-Module employs LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

-To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

6.5 Caution for operation

-It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.

-An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.

-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

6.6 Storage

In the case of storing for a long period of time, the following ways are recommended:

-Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.

-Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.

-Storing with no touch on polarizer surface by any thing else.

6.7 Safety

-It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

-When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.